SwissSEM Technologies AG

CHIP POSITION DRAWING AND THERMAL STACK
芯片位置图与热堆叠

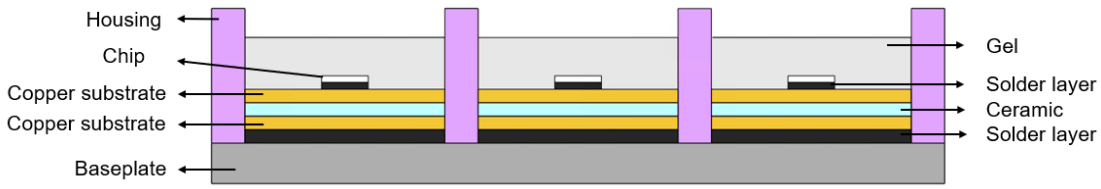
SEM AN 25-0005

Application note for SISP0100EP170i20

SISP0100EP170i20 封装模块应用说明

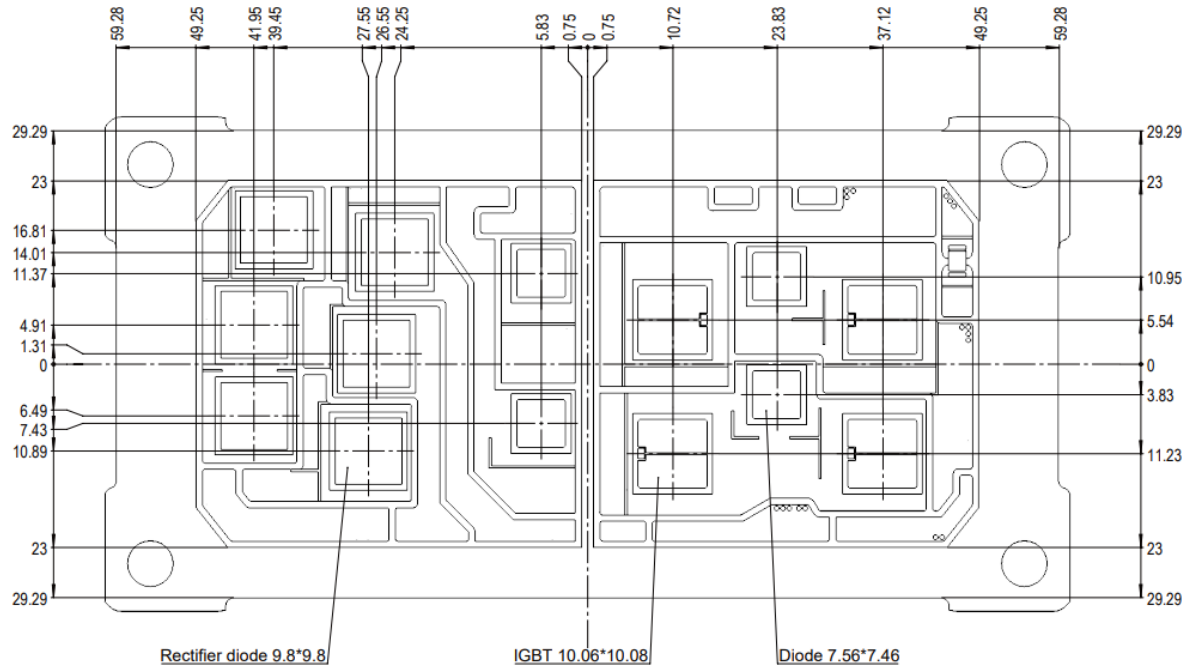
swiss semiconductors.

1 MATERIAL INFORMATION FOR EACH LAYER



	Thermal conductivity[w/(m*k)]	thickness(mm)
IGBT	147	0.185
Diode	147	0.185
Rectifier	147	0.305
Solder layer Chip- Substrate	55	0.08
Copper substrate	385	0.3
Ceramic	27	0.32
Copper substrate	385	0.3
Solder layer Substrate-Baseplate	55	0.2
Baseplate（copper）	385	3

2 CHIP POSITION



AUTHOR	CHECKED	RELEASED
R. W. R&D Engineer	R. S. VP Product Management & Application	C. T. VP Supply and Quality

3 REVISION HISTORY

DATE	AUTHOR	REMARK
Aug, 2025	R. W.	Initial version

AUTHOR	CHECKED	RELEASED
R. W. R&D Engineer	R. S. VP Product Management & Application	C. T. VP Supply and Quality